A Novel Asynchronous Integrating Latching (NAIL) deformable mirror controller

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ABSTRACT

The coronagraphs under consideration for imaging extra solar planets use deformable mirrors (DMs) to control the wavefront quality in the instrument.[1] Among the lightest and lowest power deformable mirrors are the microelectromechanical systems (MEMS) based systems.[2] Unfortunately, the current state of the art controller for such a DM is large, power inefficient, and requires an enormous interconnecting cable. While we can produce a DM the size of a sugar cube and requiring mWs of power, we require power hungry electronics the size of a bread box to run it. We are developing a chip sized DM controller. The controller is a low powered, high voltage Application Specific Integrated Circuit (ASIC). The ASIC will allow an architecture in which a single board hosts both the DM and the controller ASIC. It will be attached to the host system by a high voltage cable and a serial communications line. The concept is well suited to scale to the ever larger DMs and to the even higher precision requirements envisioned by the most ambitious missions under consideration. We describe the chip architecture and design and review its expected performance.

Keywords: instrumentation, exoplanets, direct detection, coronagraphs, deformable mirrors, control electronics

1. INTRODUCTION

No other area of scientific research has as much potential to both excite public interest and to improve our understanding of the world as the direct imaging of exoplanets. The success of indirect detection methods is breathtaking but no amount of indirect data has the public impact of an image. Likewise, the hard scientific truth that can be gleaned from light curve and radial velocity data is impressive but is far short of what can be learned by collecting light emitted or scattered by the planet.

Collecting such light and separating it from starlight requires a coronagraph. The various internal exoplanet coronagraph concepts[1,3,4] all make use of a deformable mirror (DM) to control the wavefront of the light propagating through the system. In the simplest case the DM is used to counteract the effects of the imperfections in the optics and to return the wavefront to the plane surface of light from a source many focal lengths from the aperture. This planar wavefront will focus to point spread function (PSF) with an Airy disk distribution of light and can then be attenuated by a suitable coronagraph. More advanced systems create a "dark hole" by tailoring the PSF to create regions of higher contrast.[5] In any such system, the resulting contrast, that is the ability of the coronagraph to suppress starlight, is proportional to the square of residual wavefront error left by the DM.[6,7]

Many different types of DM are available. These include piezoelectric actuators,[8] voice coil actuators,[9] and electrostatic microelectromechanical systems (MEMS) mirrors.[10] Those of interest here are the MEMS electrostatic DMs produced by Boston Micromachines Corp (BMC).[2] They are in use on the Gemini Planet Imager (GPI)[11] and other ground based systems.[12,13] They have been flown on sub-orbital[14–17] and orbital[18] missions and are being considered for Habitable Worlds Observatory (HWO).[19]

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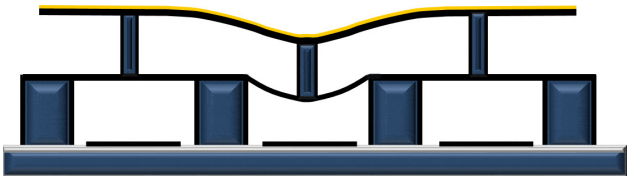

Figure 1. A MEMS DM is a capacitive device. Charge is injected onto an electrode at the bottom of the device which creates an electric field which in turn pulls the actuator and reflective face sheet down. The capacitance of the actuator represents the physical limit to the actuator performance. Note that this figure of a continuous face sheet DM, from https://bostonmicromachines.com/products/deformable-mirrors/standard-deformable-mirrors/, is greatly exaggerated in the vertical dimension. The actuators are several hundred microns horizontally and only a few microns vertically.

The BMC DMs consist of a face sheet and an array of actuators (see Figure 1). The face sheet may be a continuous membrane or it may be cut (segmented) into tiles each covering one or more actuators.[20] The facesheet is attached to the actuators by posts attached to the top of the actuators.

The actuator consists of an electrode "floor" on the lower surface, a box of rigid walls, and a flexible "roof". The floor electrode and and the roof form a parallel plate capacitor with ~ 100 fF capacitance.[21] As charge is applied to the electrode, an electric field is created between the electrode and the roof. This exerts a force on the roof and causes it to deflect, pulling on the post which, in turn, deforms the upper membrane. The membrane is metallized and acts as a mirror. To move an actuator through its full range requires 2×10^{-11} Coulombs or 1.25×10^{8} electrons.

Obviously electronics are required to control the charge on each actuator. We refer to these electronics as the DM controller. The state-of-the-art ten years ago for a controller to support a BMC 1000 actuator DM (a kilo-DM) was a 4 inch tall unit designed to be mounted in a standard 18U rack and connected to the DM through a series of flex cables. The unit drew several 10s of watts and achieved 14 bit resolution.

These flex cables are rather common across many different implementations of controllers. They results from connecting 1000 pixels on the DM to 1000 amplifiers in an entirely different location. We have rediscovered the "tyranny of numbers" problem which bedeviled early computer design.[22]

For flight, a small controller suitable for space applications was developed.[23] That controller used significantly less size, weight, and power (SWAP) than previous systems and was small enough that it could be located with the DM on the optical bench. Unfortunately, this results in a heat load (the controller power) of ~ 10 Watts into the optical bench. Furthermore, that controller depends on amplifier chips which are no longer in production. As a result, that controller can no longer be produced. More recently, a commercial-off-the-shelf (COTS) component based driver for risk tolerant missions was developed.[24] The detailed power requirements for this design are not reported but based on the general architecture an estimate of 10 to 20 watts seems reasonable.

The mass, power, and cabling required to accommodate a conventional MEMS DM controller are significant. In suborbital missions this is primarily seen in the volume and thermal requirements, in small satellites the mass and power costs are significant, while in major missions the risks associated with the extensive, delicate harnessing are a concern.

Thus is seems an appropriate time to consider the next generation controller. Previous controllers are voltage amplifier based and are limited by the bandwidth-voltage-power constraints of those amplifiers. The Novel Asynchronous Integrating Latching (NAIL) controller described here is charge based. By metering charge into the actuators NAIL only applies power as needed to move the actuator and thus operates much more efficiently at much lower power.

2. DESIGN

The key to the NAIL design is the realization that, since the DM actuators are capacitors, any charge placed on an isolated actuator will simply remain there with the actuator latched in a constant deflection. This is, of course, something of an idealization. Real world parasitic currents will cause the charge to slowly leak out

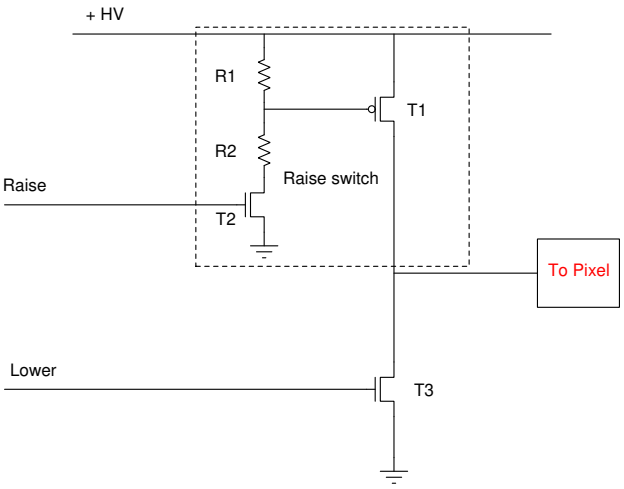

Figure 2. NAIL achieves low power by pulsing charge into and out of each pixel. To lower a pixel a switch to the high voltage bus is pulsed, letting through a small amount of charge. To raise the pixel, a switch to ground is pulsed, draining charge. The longer the pulse, the more charge.

and the actuator to relax. Fortunately, those currents are quite small and the resulting drift in deflection is manageable.

This is what NAIL does. NAIL precisely controls the charge on the actuator electrodes in order to position and shape the membrane. In operation it will receive pixel addresses and data values over a serial line from the control electronics (usually a control computer). An I/O module within the application specific integrated circuit (ASIC) will set the address on a multiplexer to access the desired pixel control line. Each pixel will have two such control lines, one to raise the pixel and one to lower it (see Figure 2). This is the integrating aspect of the NAIL control system. Charge is added or removed from the charge already in the actuator. The power applied to the pixel is only the power to move the pixel from its previous position to its next one. Since most actuator commands in operation are for very slight adjustments in position, these commands take very little power.

After addressing the correct line, the I/O module will send the data value to the selected pulse generator. The generator will form a pulse whose width is proportional to the data value. This pulse will inject charge into or drain charge out of the desired pixel (see Figure 2). NAIL is asynchronous in that any pixel can be commanded at any time in any order. As a result, pixels which need not move need not be addressed and will draw no charge and no power.

2.1 Pulse generator and resolution

This design is using the pulse width of an individual pulse to control the step size of an individual pixel. By reducing the charge injection problem to a pulse timing problem we use the very high precision and dynamic range of electronic timing circuits. The minimum size of the charge packet injected into the actuator is set by the RC time of the charging circuit and the minimum switching time of the transistor. The first NAIL ASIC will be developed with 16 bit precision. Since this is fundamentally a timing circuit higher precision is easily possible.

The pulse width is set by a counter. The desired width is written into the counter and its output remains high while the counter counts down. The counters are clocked by a precision oscillator. Drift in this oscillator will result in gain changes in the controller but high stability oscillators are common so we do not anticipate this being a significant source of error.

For a given transistor switching speed, a higher RC time constant gives more precise actuator positioning. A key modeling task in this effort will be to understand the details of the ASIC foundry process in order to optimize the high voltage transistor switching time with the internal resistance of the high voltage line (R) and the output capacitance of the ASIC (C). We can optimize both R and C to acheive the best precision and ripple characteristics given the transistor properties.

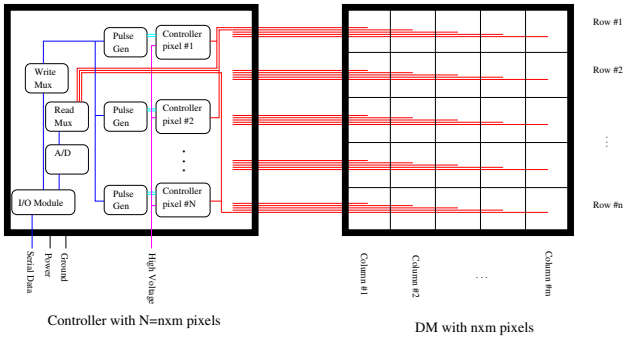

Figure 3. By implementing NAIL as a ASIC we can locate it on a printed circuit board or even in the same chip carrier as the DM. This means that the deformable mirror only needs to be connected via a USB line and a high voltage connection.

The resolution is a combination of the minimum transistor switching time and the RC time of the circuit. As with the ripple, the resolution can be improved by increasing the output capacitance. Higher output capacitance corresponds to higher resolution and higher power. The RC time, and the resolution, can also be increased by increasing the internal resistance of the high voltage line as discussed in Section 2.3. Higher resistance results in higher resolution and lower controller bandwidth.

2.2 Optimizing precision and ripple

When an actuator is not addressed the raising and lowering transistors are off and the actuator is isolated. During this time there is a small leakage current which slowly drains charge from the actuator causing the pixel to sag. This leakage is a result of the leakage current of the transistor and surface currents through any contamination on either the controller board or the DM inself. The amount of sag is related to the leakage current by the output capacitance of the controller.

In operation each pixel will need to be periodically refreshed to maintain position. Our tests show that the leakage current of an isolated BMC Multi-DM actuator results in a displacement loss of $< 63.2\%$ every 1,950 seconds, returning to 0 nm after 162.5 minutes. If each pixel is refreshed at a rate of 10 Hz, this would result in an output jitter of 0.005% of the target displacement, maintaining $> 1 : 2^{15}$ actuator positioning accuracy. This ripple can be further reduced by increasing the output capacitance of the controller. The increase can be accomplished either in chip or with small capacitors external to the device. Larger output capacitance results in lower ripple and higher power draw.

2.3 Additional design features

There are a number of extensions of the basic design which are possible to incorporate in future generations of the ASIC. Based on the lessons learned from the first generation ASIC we will incorporate these features on a best effort basis.

Voltage readback In some applications it is desirable to read back the position of the pixel through the controller. This can be accomplished by using a analog multiplexer to select a pixel to be read by an A/D converter as is shown in Figure 3. This adds some small complexity and potentially increases the leakage current.

Variable resolution As indicated in Section 2.2, the overall resolution can be increased by increasing the internal resistance of the voltage source. A series of switches can be added to increase this resistance on command. This will result in a controller with several different operating modes each with increasing precision and decreasing bandwidth.

3. EXPECTED PERFORMANCE

3.1 Resolution

The resolution is a combination of the minimum transistor switching time and the RC time of the circuit. As with the ripple, the resolution can be improved by increasing the output capacitance. Higher output capacitance corresponds to higher resolution and higher power. The RC time, and the resolution, can also be increased by increasing the internal resistance of the high voltage line as discussed in section 2.3. Higher resistance results in higher resolution and lower controller bandwidth.

The response of the DM is not linear to either voltage or charge control. $1/2^{15}$ full scale corresponds to less than 0.045 nm over 90% of the actuator's full range.

3.2 Ripple

In operation each pixel will need to be periodically refreshed to maintain position. The discharge due to the leakage current of an isolated BMC DM is well approximated by an RC decay and this corresponds to an RC time of roughly 1,950 seconds. If each pixel is refreshed at a rate of 10 Hz, this would result in an output jitter of 0.005% of the target displacement, maintaining $> 1 : 2^{15}$ actuator positioning accuracy. The pixel will dither by 1 LSB about its target displacement. This is likely to be true in any numerical control system and is explicitly true of the NAIL system.

Fortunately, the size of the LSB is entirely in the control of the designer. The ripple can be reduced by increasing the output capacitance of the controller. The frequency of the ripple is also a function of the implementation. The frequency of the ripple can be traded with the amplitude. Faster ripple corresponds to smaller amplitude.

4. IMPLEMENTATION AND STATUS

Low power is key to ASIC implementation and placing the controller proximally to the DM. It is simply not possible to run ~ 10 watts through a few mm^2 of silicon in a vacuum without damaging the device. We have calculated the expected power draw for NAIL using standard design proceedures[25] and first principle estimates. Our calculations (see figure 4) indicate that NAIL will run with an average power less than 100 mW and a peak power of about 300 mW.

We have prototyped the system[26] and have been funded for ASIC development. The ASIC design will depend on the tradeoff between transistor speed, output capacitance, and internal resistance. This trade space is currently being studied.

4.1 Device Scaling

The NAIL architecture is well suited for scaling to higher precision devices and higher pixel count actuators. The precision of NAIL is set by each pixel's charge and discharge line RC time which is in turn set by each pixel's resistance and ballast capacitor. Simply increasing the ballasting capacitance or the line resistance the RC time can be increased to raise the control precision at the cost of lowering the maximum change in displacement per unit time. The line resistance can be changed as an operating mode so that the added precision can be applied dynamically allowing faster lower precision modes followed by slower higher precision modes (see Section 2.3).

Since NAIL uses only a single counter and three high voltage transistors per actuator it is very scaleable to larger devices. In terms of ASIC area, NAIL can support far more actuators than the packaging will allow. As a result, NAIL will have the same packaging limitations as the MEMS DM and will be able to support any sized DM which can be produced. Each will be limited by the packaging. Since NAIL is a small chip several of them could be used to support a single DM further raising the pixel count. Thus it should be straightforward to support a 2K or 4K DM.

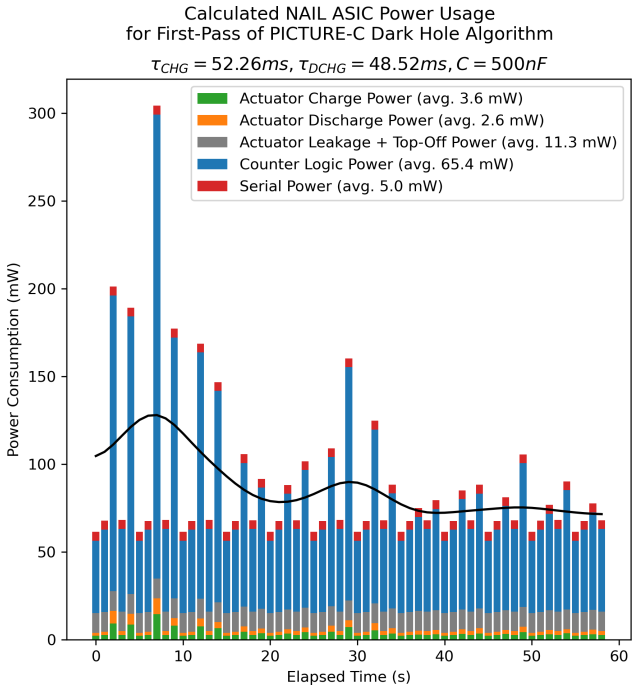

Figure 4. We have simulated the performance of NAIL in flight by modeling its response to the as-sent in-flight commanding of the PICTURE-C DM. These calculations indicate that had NAIL been available for PICTURE-C the controller would have drawn several hundred milliwatts rather than the ~ 10 watts actually dissipated by the controller. As the algorithm runs, the necessary corrections decrease in magnitude thereby further lowering the power. As shown here, the largest contributor to the power is the CMOS logic used to control the system.

5. CONCLUSION

We are developing a chip scale deformable mirror controller to support a BMC kilo-DM. By utilizing charge based control rather than traditional voltage based control, we can make the circuit much lower power. This, in turn, allows us to pack the device into a single ASIC and allows us to colocate it with the DM. This greatly reduces the SWAP of the controller and addresses the "tyranny of numbers" problem that plagues other DM controllers. It is our hope that this controller will enable a wide range of space based applications from cubesats to major missions.

6. ACKNOWLEDGEMENTS

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